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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte TAEG-HYUN KANG, JUN-HYEONG RYU,
and JONG-HWAN KIM

Appeal 2009-009003
Application 10/071,494
Technology Center 2800

Before MAHSHID D. SAADAT, MARC S. HOFF,
and ELENI MANTIS MERCADER, *Administrative Patent Judges.*

ELENI MANTIS MERCADER, *Administrative Patent Judge.*

DECISION ON APPEAL

STATEMENT OF THE CASE

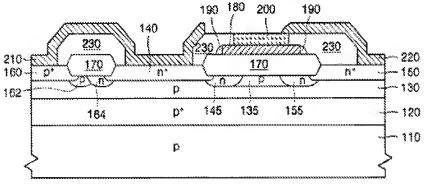
Appellants seek our review under 35 U.S.C. § 134 of the Examiner's final rejection of claims 1-10, 19-29, 40, and 41. We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

INVENTION

Appellants' Figure 2 is depicted below:

FIG. 2



Appellants' Figure 2 and claimed invention are directed to a field transistor that does not have a thin gate insulating layer. Furthermore, the entire gate conductive layer 180 is formed on the relatively-thick filed oxide layer 170 because the n^+-type source/drain regions 140 and 150 are not overlapped by the gate conductive layer 180. These two modifications over the prior art prevent dielectric destruction of an insulating layer due to

Electrostatic Discharge (ESD) Stress, thereby greatly increasing reliability of the device. *See* Spec. [08], [33].

Claim 1, reproduced below, is representative of the subject matter on appeal:

1. A field transistor having a current path between a source and a drain while containing no thin gate insulating layer, the transistor comprising:

a well region of a first conductivity type;

a field oxide layer for defining an active region on the well region;

high concentration source and drain regions of a second conductivity type separated from each other by a width of the field oxide layer;

a low concentration source region of the second conductivity type formed in the well region, the low concentration source region being adjacent to the high concentration source region and overlapped by one end of the field oxide layer;

a low concentration drain region of the second conductivity type formed in the well region, the low concentration drain region being adjacent to the high concentration drain region and overlapped by the other end of the field oxide layer; and

a gate conductive layer pattern formed on the field oxide layer, the gate conductive layer pattern overlapping parts of the low concentration source and drain regions of the second conductivity type.

THE REJECTIONS

The Examiner relies upon the following as evidence of unpatentability:

Nishida	US 3,789,503	Feb. 5, 1974
Murakami	US 5,623,154	Apr. 22, 1997
Hsu	US 6,841,821 B2	Jan. 11, 2005

The following rejections are before us for review:

1. Claims 1-10, 19-29, 40, and 41 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

2. Claims 1-4, 7-10, 19, 23, 26, 27, and 29 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Murakami.

ISSUES

The pivotal issues are:

1. whether one skilled in the art would know what the dimensions are of a "thin gate insulating layer"; and

2. whether the Examiner erred in not addressing the limitation of "*no* thin gate insulating layer" (emphasis added).

PRINCIPLES OF LAW

> [T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application. "[C]ustomary meaning" refers to the "customary meaning in [the] art field."

Phillips v. AWH Corp., 415 F.3d 1303, 1313 (Fed. Cir. 2005) (second brackets in original) (citations omitted).

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior

art reference." *Verdegaal Bros., Inc., v. Union Oil Co. of Cal.*, 814 F.2d 628, 631 (Fed. Cir. 1987).

ANALYSIS

Analysis with respect to the rejection of claims 1-10, 19-29, 40, and 41 under 35 U.S.C. § 112, second paragraph

Appellants argue that (App. Br. 14-15 (citing MPEP § 2173.05(b))) a skilled artisan at the time of the invention would have been reasonably apprised of the scope of the "thin gate oxide layer" or "thin gate insulating layer."

We are persuaded by Appellants' argument. The customary meaning in the art of the claim term "thin gate oxide layer" or "thin gate insulating layer" *at the time of the invention* can be readily determined by the cited reference of Hsu.[1] Hsu discloses that the thin gate oxide layer has a thickness of 1.5-6 nanometers (nm) (col. 2, ll. 56-58) or 15-60 Angstroms (Final Rej. 2, as converted into Angstrom units by the Examiner). *See Phillips*, 415 F.3d at 1313. Thus, one skilled in the art would readily recognize the term "thin gate oxide layer" would refer to a thickness on the order of tens of Angstroms.

[1] Hsu '821 has an effective filling date of October 7, 1999. The original application of Hsu (now U.S. patent 6,457,108), of which Hsu '821 is a continuation in part (CIP), also includes the cited part (in Hsu '108 the same portion appears in col. 2, ll. 49-51) relied upon by the Examiner in the Final Rejection (Final Rej. 2 citing a thickness of 15-60 Angstroms).

We are not persuaded by the Examiner's response that one skilled in the art would not know the dimensions of a "thin gate oxide layer" because there is a difference of almost 1600 Angstroms between the Nishida patent published in 1974 and the Hsu patent issued in 2005. As our reviewing Court decided, customary art definitions are determined as of *the time of the invention*. *See Phillips*, 415 F.3d at 1313.

Thus, one skilled in the art would look at the Hsu patent for guidance to determine the "thin gate oxide layer" dimensions. We also agree with Appellants (App. Br. 16) that a skilled artisan would not look to Nishida for guidance for dimensions because the size and dimensions of semiconductor devices have been decreasing over the years.

Thus, we will reverse the Examiner's rejection of claims 1-10, 19-29, 40, and 41 under 35 U.S.C. § 112, second paragraph.

Analysis with respect to the rejection of claims 1-4, 7-10, 19, 23, 26, 27, and 29 under 35 U.S.C. § 102(b) as being anticipated by Murakami

Appellants argue (App. Br. 20) that the Examiner gave no weight to the limitation of "*no* thin gate insulating layer."

We are persuaded by Appellants' arguments. We do not agree with the Examiner's reasoning (Ans. 13) that there is no structural difference from the device taught by Murakami because of the indefiniteness rejection of the limitation. The Examiner still has the burden to address such a limitation under the art rejection. A claim limitation that is considered indefinite cannot be disregarded; instead, the limitation should also be rejected over the prior art based on the interpretation of the claim that

renders the prior art applicable. *See* MPEP § 2143.03(I); *Ex parte Ionescu*, 222 USPQ 537 (BPAI 1984).

Furthermore, we note that the Examiner also ignored the limitation of "a gate conductive layer pattern formed on the field oxide layer." One skilled in the art would have readily recognized that the field oxide layer in Murakami is layer 5 (*see* Fig. 13), and as such, Murakami does not teach "a gate conductive layer pattern formed on the field oxide layer" because there is no gate conductive layer *on* the field oxide layer 5.

Thus, we will also reverse the Examiner's rejections of claims 1-4, 7-10, 19, 23, 26, 27, and 29 under 35 U.S.C. § 102(b).

CONCLUSIONS

1. One skilled in the art would know the dimensions of a "thin gate insulating layer."

2. The Examiner erred in not addressing the limitation of "*no* thin gate insulating layer" (emphasis added).

ORDER

The decision of the Examiner to reject claims 1-10, 19-29, 40, and 41 is reversed.

REVERSED

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